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L14: (14) 11 and 13 | US 4780891 A | Tag: S | Doc: 13/14

	Document ID	Kind Codes	Source	Issue Date	Pa
1	US 5652668 A		USPAT	19970729	20
2	US 5631759 A		USPAT	19970520	20
3	US 5617238 A		USPAT	19970401	21
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13	US 4780891 A		USPAT	19881025	11
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Details | Text | Image | HTML

L14: (14) 11 and 13 | US 4780891 | Tag: S | Doc: 13/14 | "Full" 6/11 (Total images 11)

Arial 12

1. Field of the Invention

The invention concerns synchronization of synchronous digital bit streams.

2. Description of the Prior Art

It is known to transmit information over a line in the form of a binary bit stream and processing of the information often entails reading the binary bit stream by means of the associated clock signal. This reading is generally effected by means of a D type flip-flop. The information is read on the rising or falling edge of the clock signal driving the flip-flop and passed to the output of the flip-flop. For the reading to be effected correctly the information has to be present for at least a setup time before the active (rising or falling) edge of the clock signal and for at least a hold time after this edge.

When there is more than one bit stream, each bit stream being transmitted by a respective line, the bit streams are made synchronous, in accordance with CCITT Recommendation G. 701, when their significant instants occur at exactly the same rate on average, the bit streams possibly being affected by amplitude jitter lying between specified limits.

It is therefore possible to read synchronous digital bit streams by means of a common clock signal running at the rate at which the significant instants of the bit streams occur, provided that the conditions in respect of setup and hold times are respected. As a general rule these conditions do not raise any problem when the information is at a low bit rate. On the other hand, it becomes necessary to synchronize the bit streams when the hold and setup times and the spread in propagation time in the logic circuits and amplifiers sending the bit streams and in the transmission lines are no longer negligible in comparison with the bit duration, in other words when the bit streams have a high bit rate.

An object of the invention is to synchronize synchronous digital bit streams, in particular to enable them to be read by a common clock signal.

SUMMARY OF THE INVENTION

In one aspect, the invention consists in a method of synchronizing synchronous digital bit streams each comprising bits each having the same bit duration, wherein one of said bit streams is taken as a reference and provides a basis for defining successive reference time intervals each equal to said bit duration, a plurality of timing windows are defined within each reference time interval, a second bit stream is subjected to a time-delay that may have a null or zero value, one of said windows is taken as a reference window on the basis of a required phase relationship between said reference bit stream and said second bit stream, the phases of said reference bit stream and said second bit stream are compared using said reference digital bit stream, a phase compara... connected to said timing window generator, a ti... delay selector connected to said phase comparator... switching device, an input of said switching dev... connected to said time-delay selector, a plurality ... time-delay circuits each imposing a respective ti... delay which is a multiple of a common basic time-de... adapted to be connected to a second line carrying ... second digital bit stream before it is subjected to a ... time-delay, a plurality of inputs of said switching dev... adapted to be connected to said second line and to a ... time-delay devices, the number of inputs of said swit... ing device being one greater than the number of ... time-delay circuits, an output of said switching dev... adapted to be connected to a third line carrying ... second bit stream after it is subjected to said time-del... and an input of said phase comparator adapted to ... connected to said third line.

The method in accordance with the invention ... quires that the synchronous digital bit streams comp... a minimum number of transitions, a condition whic... generally met when they are from an optical or coa... line terminal comprising a limited sum encoder ... scrambler.

Other objects and advantages will appear from ... following description of examples of the inventi... when considered in connection with the accompany... drawings, and the novel features will be particula... pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a device in accordan... with the invention for synchronizing two bit stream...

FIG. 2 is a diagram showing timing windows as ... fined by a circuit from FIG. 1.

FIG. 3 shows one example of the method of synch... nizing two digital bit streams.

FIG. 4 shows another example of the method of s... chronizing two digital bit streams.

FIG. 5 represents a state diagram relating to FIG...

FIG. 6 represents a state diagram relating to FIG...

FIG. 7 shows one embodiment of the device in acc... dance with the invention.

FIG. 8 shows another embodiment of the devic... accordance with the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the device shown in block diagram form in FIG... two lines 1 and 2 carry respective synchronous dig... bit streams A and B each with the same bit duration... time-delay devices LR1 through LRn have their in... connected to line 2 and their output connected t... switching device 3; line 2 is also connected direct to ...

Details | Text | Image | HTML | Full

Ready NUM

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United States Patent [19]

Pederson

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[45] Date of Patent: Apr. 28, 1992

[54] METHOD OF APPARATUS FOR DETECTING DEFECTS IN DATA APPARATUS SUCH AS MAGNETIC STORAGE APPARATUS

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[21] Appl. No.: 445,043

[22] Filed: Dec. 4, 1989

[51] Int. Cl.[5] G11B 5/09

[52] U.S. Cl. 360/51

[58] Field of Search 360/51, 46, 45, 31

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Primary Examiner—Vincent P. Canney
Attorney, Agent, or Firm—Curtis, Morris & Safford

[57] ABSTRACT

A technique is provided for detecting defects in data apparatus, such as magnetic storage apparatus, wherein recovered data pulses are expected during periodic window intervals. Data pulses which may be phase shifted relative to predetermined data pulse times of occurrence are recovered, such as by playing back such pulses from a magnetic storage medium, for example, a hard disk drive. The recovered data pulses are selectively delayed, and the delayed and undelayed data pulses are multiplexed into a stream. The occurrences of such data pulses in the stream within the aforementioned window intervals are detected to provide indications of defects. A defect is indicated if a pulse in the stream does not occur within the window interval.

27 Claims, 3 Drawing Sheets